IN THE ABSTRACT:

Please replace the original Abstract of the Disclosure with the attached Abstract of the Disclosure.

IN THE CLAIMS:

Please cancel claim 3 without prejudice to or disclaimer of the subject matter contained therein.

Please replace the text of claims 1, 4-9 and 13 with the following text:

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1. A semiconductor device comprising:

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a dicing region provided on a semiconductor substrate to separate a plurality of semiconductor chips each having a gate portion from each other;

a plurality of element isolation regions provided on a surface portion of the semiconductor substrate within the dicing region;

a plurality of first dummy patterns formed on a surface of the semiconductor substrate so as to correspond to intervals of the plurality of element isolation regions, respectively; and

a plurality of second dummy patterns formed above the semiconductor substrate within the dicing region so as to correspond to the plurality of first dummy patterns, respectively.

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4. The semiconductor device according to claim 1, wherein the plurality of first dummy patterns each have a structure which is substantially similar to that of the gate potion.

5. The semiconductor device according to claim 4, wherein the plurality of first dummy patterns and the gate portions each have a laminated structure including a gate oxide film, a polysilicon film, a WSi film, and a SiN film.

6. The semiconductor device according to claim 1, wherein the plurality of element isolation regions each have an STI structure.

7. The semiconductor device according to claim 1, wherein the plurality of first dummy patterns and the element isolati n regions are arranged alternately to form a predetermined repetitive pattern.

A3 Concl'd

8. The semiconductor device according to claim 1, wherein the plurality of second dummy patterns include at least protection films provided on the surface of the semiconductor substrate.

9. The semiconductor device according to claim 8, wherein the plurality of second dummy patterns include insulation films provided on the surface of the semiconductor substrate.

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12. The semiconductor device according to claim 1, wherein the plurality of first dummy patterns and the plurality of second dummy patterns are formed along the dicing region.

REMARKS

The Office Action mailed October 4, 2002, has been carefully reviewed and the foregoing amendments and the following remarks are made in response thereto.

The Office Action requires a new title that is clearly indicative of the invention to which the claims are directed. The specification and the claims stand objected to for minor informalities. Claims 1-3 and 10-13[1] stand rejected under 35 U.S.C. 102(a) as being anticipated by U.S. Patent No. 5,763,936 to Yamaha et al. (hereinafter "Yamaha"). Claims 4 and 5 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaha in view of Applicants' Admitted Prior Art (hereinafter "AAPA") and claims 6 and 7 stand rejected under the same as being unpatentable over Yamaha in view of U.S. Patent No. 5,414,297 to Morita.

By this amendment, the specification has been amended to address the Examiner's concerns. In particular, the Office Action asserts that the title of the application was not descriptive. Applicants have amended the title to overcome this objection. It is respectfully

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[1] The Examiner indicates on page 3 of the Office Action that only claims 1-3 and 10-13 are rejected under 35 U.S.C. 102(a) as being anticipated by Yamaha. However, on page 4 of the Office Action, the Examiner provides a rejection for claims 8 and 9 as being anticipated by Yamaha. Since the Office Action Summary indicates that claims 1-13 have been rejected, Applicants will assume that the Examiner meant to include the rejection of claims 8 and 9 on page 3 of this Office Action.